Amendments to the Claims:

Claims 9 and 25-30 have been amended and new claims 31-40 have been added. This listing of the claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

(Claims 1-8 have been cancelled)

9.(Currently Amended) A microprocessor, comprising:

a central processing unit with an instruction set including three-byte instructions;

a memory for storing the instructions, wherein the instructions are stored contiguously; and

a memory interface for supplying the instructions from the memory to the central processing unit, wherein all bytes of each of said instructions ~~is~~ are supplied simultaneously in a single fetch operation.

10.(Original) The microprocessor of claim 9, wherein said instruction set further includes two-byte instructions and one-byte instructions.

11.(Original) The microprocessor of claim 9, wherein said memory is a one time programmable memory.

12.(Original) The microprocessor of claim 9, wherein said memory interface comprises a bus on which the instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

(Claims 13-24 have been cancelled)

25.(Currently Amended) A method of operating a microprocessor, the microprocessor comprising a central processing unit with an instruction set including N-byte instructions, a memory for storing the instructions, and a memory interface for supplying the instructions from the memory to the central processing unit, wherein N is an integer greater than one, the method comprising:

logically organizing the memory as a plurality rows of M byte-wide columns, wherein M is an integer greater than one and wherein N and M are relatively prime;

programming the instruction set into the memory, wherein the instructions are stored contiguously in the memory; and

operating the interface whereby each of the instructions can be supplied from the memory to the central processing unit in a single fetch operation.

26.(Currently Amended) The ~~microprocessor~~ method of claim 25, wherein N is equal to three and M is equal to four.

27.(Currently Amended) The ~~microprocessor~~ method of claim 26, wherein said instruction set further includes two byte instructions and one byte instructions.

28.(Currently Amended) The ~~microprocessor~~ method of claim 26, wherein said memory interface comprises a bus on which the instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

29.(Currently Amended) The ~~microprocessor~~ method of claim 25, wherein the memory is an embedded memory of the microprocessor.

30.(Currently Amended) The ~~microprocessor~~ method of claim 29, wherein the memory is a one time programmable memory.

31.(New) The microprocessor of claim 9, wherein said memory is four bytes wide.

32.(New) The microprocessor of claim 10, wherein said memory is a one time programmable memory.

33.(New) The microprocessor of claim 10, wherein said memory interface comprises a bus on which the instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

34.(New) A microprocessor, comprising:

a central processing unit operable according to an instruction set including instructions of one-byte, two-byte, and three-byte lengths;

a memory for storing said instructions, wherein all of the members of the instruction set are stored contiguously; and

a memory interface for supplying instructions of the instruction set from the memory to the central processing unit, wherein each of said instructions is individually suppliable in a single fetch operation in which all bytes of a supplied instruction are supplied simultaneously.

35.(New) The microprocessor of claim 34, wherein said memory is organized as a plurality rows of M byte-wide columns, wherein M is an integer greater than three that is not divisible by three.

36.(New) The microprocessor of claim 34, wherein said memory is a one time programmable memory.

37.(New) The microprocessor of claim 34, wherein said memory interface comprises a bus on which the instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

38.(Original) The method of claim 27, wherein said memory interface comprises a bus on which the instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

39.(Original) The method of claim 27, wherein the memory is an embedded memory of the microprocessor.

40.(Original) The method of claim 39, wherein the memory is a one time programmable memory.